What is claimed is:

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1. A messaging mechanism for inter-processor communication comprising:

a shared service processor providing a single point of contact for a user interfacing with at least one line processor, the service processor in electrical communication with shared memory including mailboxes operable to enable communication between the at least one line processor and the service processor; wherein

the service processor is operable to selectively deliver commands to a respective mailbox of a selected one of said at least one line processsor, and

the service processor is selectively operable to issue a system management interrupt to any or all of the at least one line processors, the interrupt signaling to the at least one line processor to access a respective mailbox in the shared memory.

2. The messaging mechanism of claim 1, wherein the line processor receiving the system management interrupt will access the command delivered to the respective mailbox, interpret the command and deliver an appropriate response to a mailbox.

3. The messaging mechanism of claim 2, wherein the line processor is operable to assert its system management interrupt line to the service processor after delivering the appropriate response to the mailbox.

4. The messaging mechanism of claim 1, wherein said shared service processor further is electrically interconnected to nonvolatile memory for storing initialization and/or boot information for the service processor and at least one line processor.

5. The messaging mechanism of claim 1 wherein the at least one line processor is operable to conserve backplane bandwidth by selectively consolidating selected tasks onto the service processor to reduce the number of accesses to a backplane to which the service processor and the at least one line processor are coupled.

6. A method for inter-processor communication messaging comprising the steps of:

providing a shared processor serving as a single point of contact for a user interfacing with at least one line processor,

providing mailboxes for each of the at least one line processors and the shared processor enabling communication between the at least one line processor and the shared processor;

selectively delivering commands from the shared processor to a respective mailbox of a selected one of said at least one line processor, and

selectively issuing a system management interrupt from the shared processor to any or all of the at least one line processors, the interrupt signaling to the at least one line processor to access a respective mailbox in the shared memory.

7. The messaging method of claim 6, further comprising the step of:

causing the at least one line processor to access, in response to a system management interrupt, the respective mailbox, interpret the command and deliver the appropriate response to a mailbox.

8. The messaging mechanism of claim 7, further comprising the step of:

causing the at least one line processor to assert its system management interrupt line to the shared processor to indicate that said response has been delivered.

9. A messaging mechanism for inter-processor communication comprising:

a shared service processor providing a single point of contact for a user interfacing with at least one line processor, the shared processor in electrical communication with shared memory including mailboxes operable to enable communication between the at least one line processor and the service processor; wherein

the service processor is operable to selectively deliver commands to a respective mailbox of a selected one of said at least one line processor,

the service processor is selectively operable to issue a system management interrupt to any or all of the at least one line processors, the interrupt signaling to the at least one line processor to access a respective mailbox in the shared memory;

the at least one line processor operable to selectively deliver commands to mailboxes, wherein the commands delivered to the mailboxes by the at least one line processor are consolidated by the service processor to reduce the number of accesses to a backplane to which the service processor and the at least one line processor are coupled.